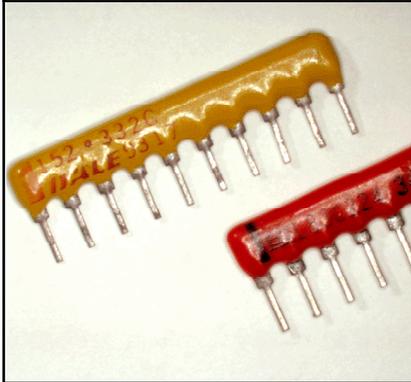


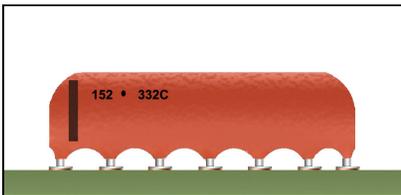
**THROUGH-HOLE SOLDERING
SINGLE IN-LINE PACKAGE / SIP**



SINGLE IN-LINE PACKAGE (SIP)

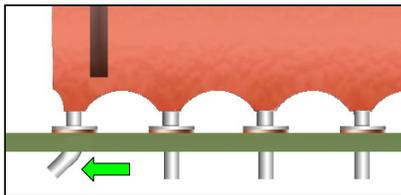
Single In-Line Package (SIP) components have a flat body oriented vertically to the printed wiring board and a single row of pins or leads. Most small-form SIPs are parallel-array devices of common value components (i.e.: diode, resistor arrays). Large-form SIPs are usually hybrid circuits (i.e. timers, oscillators, etc.). The SIP body can be either plastic or ceramic with between 4 to 64 leads.

See Section 6.01 "Through-Hole Soldering, General Requirements", for common accept / reject criteria.



PREFERRED

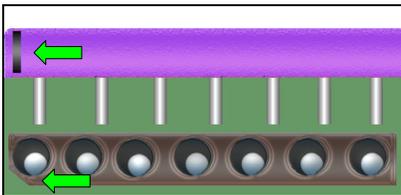
The component has been properly oriented and all leads are fully inserted in the termination holes with the lead standoff step in contact with the lands. The component body is undamaged and part markings are legible and visible.



**ACCEPTABLE
PARTIALLY CLINCHED LEADS**

The end leads may be partially clinched to temporarily secure the component. Clinching shall not violate minimum electrical spacing requirements, or adversely affect solderability.

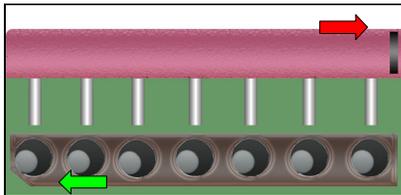
[Best Workmanship Practice](#)



**ACCEPTABLE
ORIENTATION / POLARITY**

The component has been properly installed. The chip's notch / paint stripe, which identifies pin 1, is lined up with the silkscreen pattern. A square-shaped solder pad on the printed wiring pattern may also be used to identify pin 1.

[NASA-STD-8739.3 \[8.1 \]](#)



**UNACCEPTABLE
IMPROPER ORIENTATION / POLARITY**

The SIP has been installed backwards. The locator notch / dimple, which identifies pin 1 of the chip, should be lined up to the silkscreen and/or conductive pattern marks.

[NASA-STD-8739.3 \[13.6.2.a.5 \]](#)

NASA WORKMANSHIP STANDARDS



NATIONAL AERONAUTICS AND
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JOHNSON SPACE CENTER
HOUSTON, TEXAS USA 77058

Released:
06.27.2002

Revision:

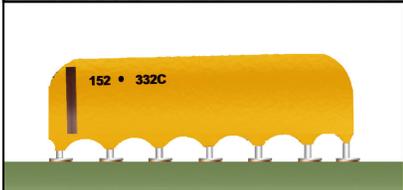
Revision Date:

Book:
6

Section:
6.12

Page:
1

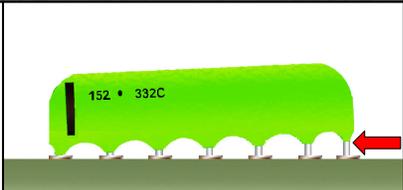
**THROUGH-HOLE SOLDERING
SINGLE IN-LINE PACKAGE / SIP (cont.)**



**ACCEPTABLE
TILT**

The component exhibits minor tilting, but the tilt does not reduce lead protrusion below acceptable minimums, cause the component body to exceed height requirements, or violate minimum electrical spacing requirements.

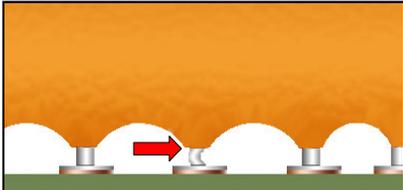
[NASA-STD-8739.3 \[8.1 \]](#), [\[13.6.1 \]](#)



**UNACCEPTABLE
EXCESS TILT**

Excess part tilt causes the leads to not meet minimum protrusion requirements. Excess tilt may cause the part to exceed maximum height requirements, or result in violation of minimum electrical clearance requirements.

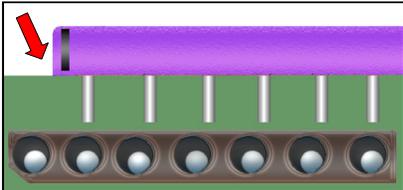
[NASA-STD-8739.3 \[13.6.2.a.21 \]](#)



**UNACCEPTABLE
BENT / CURLED LEAD**

The lead has been smashed into the pad surface, preventing proper insertion. This may be caused by improper lead planarity, an improperly bent lead, or a solder-plugged hole.

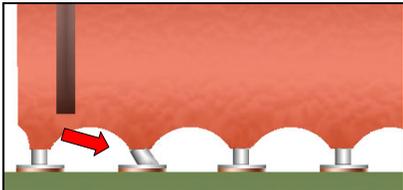
[NASA-STD-8739.3 \[13.6.2.a.7 \]](#), [\[13.6.2.a.21 \]](#)



**UNACCEPTABLE
IMPROPER ORIENTATION / OFFSET**

The component has been incorrectly installed, with the chip offset with respect to the intended termination pattern.

[NASA-STD-8739.3 \[13.6.2.a.5 \]](#)



**UNACCEPTABLE
PISTONED LEAD**

The lead has been displaced vertically (pistoned) during insertion. This may be caused by improper lead planarity, an improperly bent lead, or a solder-plugged hole.

[NASA-STD-8739.3 \[13.6.2.a.7 \]](#), [\[13.6.2.a.21 \]](#)

NASA WORKMANSHIP STANDARDS

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